

# LOW POWER SCAN & DELAY TEST METHOD AND APPARATUS

## CROSS-REFERENCE TO RELATED APPLICATIONS

The disclosure extends upon and incorporates herein by reference patent Application Number 09/803,588, filed March 9, 2001 "Adapting Scan Architectures for Low Power Operation", and patent Application Number 09/803,608, filed March 9, 2001 "Adapting Scan-BIST Architectures for Low Power Operation".

## BACKGROUND OF THE INVENTION

### FIELD OF THE INVENTION

Serial scan and Scan-BIST(Built In Self Test) architectures are commonly used to test digital circuitry in integrated circuits. The present invention improves upon the previously described low power Scan and Scan-BIST methods. These previously described methods use split scan paths to reduce power consumption. The disclosed improvement provides for the referenced low power Scan and Scan-BIST architectures to achieve a delay test capability equally as effective as the delay test capabilities used in conventional scan and Scan-BIST architectures. A delay test captures a response from the logic circuit a clock time after application of a stimulus.

### DESCRIPTION OF RELATED ART

In Figure 1, a circuit 100 includes a conventional scan architecture configured for a test. In the normal functional configuration, circuit 100 may be a functional

09/803,588  
09/803,608  
09/803,589  
09/803,609  
09/803,610  
09/803,611  
09/803,612  
09/803,613  
09/803,614  
09/803,615  
09/803,616  
09/803,617  
09/803,618  
09/803,619  
09/803,620  
09/803,621  
09/803,622  
09/803,623  
09/803,624  
09/803,625  
09/803,626  
09/803,627  
09/803,628  
09/803,629  
09/803,630  
09/803,631  
09/803,632  
09/803,633  
09/803,634  
09/803,635  
09/803,636  
09/803,637  
09/803,638  
09/803,639  
09/803,640  
09/803,641  
09/803,642  
09/803,643  
09/803,644  
09/803,645  
09/803,646  
09/803,647  
09/803,648  
09/803,649  
09/803,650  
09/803,651  
09/803,652  
09/803,653  
09/803,654  
09/803,655  
09/803,656  
09/803,657  
09/803,658  
09/803,659  
09/803,660  
09/803,661  
09/803,662  
09/803,663  
09/803,664  
09/803,665  
09/803,666  
09/803,667  
09/803,668  
09/803,669  
09/803,670  
09/803,671  
09/803,672  
09/803,673  
09/803,674  
09/803,675  
09/803,676  
09/803,677  
09/803,678  
09/803,679  
09/803,680  
09/803,681  
09/803,682  
09/803,683  
09/803,684  
09/803,685  
09/803,686  
09/803,687  
09/803,688  
09/803,689  
09/803,690  
09/803,691  
09/803,692  
09/803,693  
09/803,694  
09/803,695  
09/803,696  
09/803,697  
09/803,698  
09/803,699  
09/803,700  
09/803,701  
09/803,702  
09/803,703  
09/803,704  
09/803,705  
09/803,706  
09/803,707  
09/803,708  
09/803,709  
09/803,710  
09/803,711  
09/803,712  
09/803,713  
09/803,714  
09/803,715  
09/803,716  
09/803,717  
09/803,718  
09/803,719  
09/803,720  
09/803,721  
09/803,722  
09/803,723  
09/803,724  
09/803,725  
09/803,726  
09/803,727  
09/803,728  
09/803,729  
09/803,730  
09/803,731  
09/803,732  
09/803,733  
09/803,734  
09/803,735  
09/803,736  
09/803,737  
09/803,738  
09/803,739  
09/803,740  
09/803,741  
09/803,742  
09/803,743  
09/803,744  
09/803,745  
09/803,746  
09/803,747  
09/803,748  
09/803,749  
09/803,750  
09/803,751  
09/803,752  
09/803,753  
09/803,754  
09/803,755  
09/803,756  
09/803,757  
09/803,758  
09/803,759  
09/803,760  
09/803,761  
09/803,762  
09/803,763  
09/803,764  
09/803,765  
09/803,766  
09/803,767  
09/803,768  
09/803,769  
09/803,770  
09/803,771  
09/803,772  
09/803,773  
09/803,774  
09/803,775  
09/803,776  
09/803,777  
09/803,778  
09/803,779  
09/803,780  
09/803,781  
09/803,782  
09/803,783  
09/803,784  
09/803,785  
09/803,786  
09/803,787  
09/803,788  
09/803,789  
09/803,790  
09/803,791  
09/803,792  
09/803,793  
09/803,794  
09/803,795  
09/803,796  
09/803,797  
09/803,798  
09/803,799  
09/803,800  
09/803,801  
09/803,802  
09/803,803  
09/803,804  
09/803,805  
09/803,806  
09/803,807  
09/803,808  
09/803,809  
09/803,810  
09/803,811  
09/803,812  
09/803,813  
09/803,814  
09/803,815  
09/803,816  
09/803,817  
09/803,818  
09/803,819  
09/803,820  
09/803,821  
09/803,822  
09/803,823  
09/803,824  
09/803,825  
09/803,826  
09/803,827  
09/803,828  
09/803,829  
09/803,830  
09/803,831  
09/803,832  
09/803,833  
09/803,834  
09/803,835  
09/803,836  
09/803,837  
09/803,838  
09/803,839  
09/803,840  
09/803,841  
09/803,842  
09/803,843  
09/803,844  
09/803,845  
09/803,846  
09/803,847  
09/803,848  
09/803,849  
09/803,850  
09/803,851  
09/803,852  
09/803,853  
09/803,854  
09/803,855  
09/803,856  
09/803,857  
09/803,858  
09/803,859  
09/803,860  
09/803,861  
09/803,862  
09/803,863  
09/803,864  
09/803,865  
09/803,866  
09/803,867  
09/803,868  
09/803,869  
09/803,870  
09/803,871  
09/803,872  
09/803,873  
09/803,874  
09/803,875  
09/803,876  
09/803,877  
09/803,878  
09/803,879  
09/803,880  
09/803,881  
09/803,882  
09/803,883  
09/803,884  
09/803,885  
09/803,886  
09/803,887  
09/803,888  
09/803,889  
09/803,890  
09/803,891  
09/803,892  
09/803,893  
09/803,894  
09/803,895  
09/803,896  
09/803,897  
09/803,898  
09/803,899  
09/803,900  
09/803,901  
09/803,902  
09/803,903  
09/803,904  
09/803,905  
09/803,906  
09/803,907  
09/803,908  
09/803,909  
09/803,910  
09/803,911  
09/803,912  
09/803,913  
09/803,914  
09/803,915  
09/803,916  
09/803,917  
09/803,918  
09/803,919  
09/803,920  
09/803,921  
09/803,922  
09/803,923  
09/803,924  
09/803,925  
09/803,926  
09/803,927  
09/803,928  
09/803,929  
09/803,930  
09/803,931  
09/803,932  
09/803,933  
09/803,934  
09/803,935  
09/803,936  
09/803,937  
09/803,938  
09/803,939  
09/803,940  
09/803,941  
09/803,942  
09/803,943  
09/803,944  
09/803,945  
09/803,946  
09/803,947  
09/803,948  
09/803,949  
09/803,950  
09/803,951  
09/803,952  
09/803,953  
09/803,954  
09/803,955  
09/803,956  
09/803,957  
09/803,958  
09/803,959  
09/803,960  
09/803,961  
09/803,962  
09/803,963  
09/803,964  
09/803,965  
09/803,966  
09/803,967  
09/803,968  
09/803,969  
09/803,970  
09/803,971  
09/803,972  
09/803,973  
09/803,974  
09/803,975  
09/803,976  
09/803,977  
09/803,978  
09/803,979  
09/803,980  
09/803,981  
09/803,982  
09/803,983  
09/803,984  
09/803,985  
09/803,986  
09/803,987  
09/803,988  
09/803,989  
09/803,990  
09/803,991  
09/803,992  
09/803,993  
09/803,994  
09/803,995  
09/803,996  
09/803,997  
09/803,998  
09/803,999  
09/803,1000  
09/803,1001  
09/803,1002  
09/803,1003  
09/803,1004  
09/803,1005  
09/803,1006  
09/803,1007  
09/803,1008  
09/803,1009  
09/803,1010  
09/803,1011  
09/803,1012  
09/803,1013  
09/803,1014  
09/803,1015  
09/803,1016  
09/803,1017  
09/803,1018  
09/803,1019  
09/803,1020  
09/803,1021  
09/803,1022  
09/803,1023  
09/803,1024  
09/803,1025  
09/803,1026  
09/803,1027  
09/803,1028  
09/803,1029  
09/803,1030  
09/803,1031  
09/803,1032  
09/803,1033  
09/803,1034  
09/803,1035  
09/803,1036  
09/803,1037  
09/803,1038  
09/803,1039  
09/803,1040  
09/803,1041  
09/803,1042  
09/803,1043  
09/803,1044  
09/803,1045  
09/803,1046  
09/803,1047  
09/803,1048  
09/803,1049  
09/803,1050  
09/803,1051  
09/803,1052  
09/803,1053  
09/803,1054  
09/803,1055  
09/803,1056  
09/803,1057  
09/803,1058  
09/803,1059  
09/803,1060  
09/803,1061  
09/803,1062  
09/803,1063  
09/803,1064  
09/803,1065  
09/803,1066  
09/803,1067  
09/803,1068  
09/803,1069  
09/803,1070  
09/803,1071  
09/803,1072  
09/803,1073  
09/803,1074  
09/803,1075  
09/803,1076  
09/803,1077  
09/803,1078  
09/803,1079  
09/803,1080  
09/803,1081  
09/803,1082  
09/803,1083  
09/803,1084  
09/803,1085  
09/803,1086  
09/803,1087  
09/803,1088  
09/803,1089  
09/803,1090  
09/803,1091  
09/803,1092  
09/803,1093  
09/803,1094  
09/803,1095  
09/803,1096  
09/803,1097  
09/803,1098  
09/803,1099  
09/803,1100  
09/803,1101  
09/803,1102  
09/803,1103  
09/803,1104  
09/803,1105  
09/803,1106  
09/803,1107  
09/803,1108  
09/803,1109  
09/803,1110  
09/803,1111  
09/803,1112  
09/803,1113  
09/803,1114  
09/803,1115  
09/803,1116  
09/803,1117  
09/803,1118  
09/803,1119  
09/803,1120  
09/803,1121  
09/803,1122  
09/803,1123  
09/803,1124  
09/803,1125  
09/803,1126  
09/803,1127  
09/803,1128  
09/803,1129  
09/803,1130  
09/803,1131  
09/803,1132  
09/803,1133  
09/803,1134  
09/803,1135  
09/803,1136  
09/803,1137  
09/803,1138  
09/803,1139  
09/803,1140  
09/803,1141  
09/803,1142  
09/803,1143  
09/803,1144  
09/803,1145  
09/803,1146  
09/803,1147  
09/803,1148  
09/803,1149  
09/803,1150  
09/803,1151  
09/803,1152  
09/803,1153  
09/803,1154  
09/803,1155  
09/803,1156  
09/803,1157  
09/803,1158  
09/803,1159  
09/803,1160  
09/803,1161  
09/803,1162  
09/803,1163  
09/803,1164  
09/803,1165  
09/803,1166  
09/803,1167  
09/803,1168  
09/803,1169  
09/803,1170  
09/803,1171  
09/803,1172  
09/803,1173  
09/803,1174  
09/803,1175  
09/803,1176  
09/803,1177  
09/803,1178  
09/803,1179  
09/803,1180  
09/803,1181  
09/803,1182  
09/803,1183  
09/803,1184  
09/803,1185  
09/803,1186  
09/803,1187  
09/803,1188  
09/803,1189  
09/803,1190  
09/803,1191  
09/803,1192  
09/803,1193  
09/803,1194  
09/803,1195  
09/803,1196  
09/803,1197  
09/803,1198  
09/803,1199  
09/803,1200  
09/803,1201  
09/803,1202  
09/803,1203  
09/803,1204  
09/803,1205  
09/803,1206  
09/803,1207  
09/803,1208  
09/803,1209  
09/803,1210  
09/803,1211  
09/803,1212  
09/803,1213  
09/803,1214  
09/803,1215  
09/803,1216  
09/803,1217  
09/803,1218  
09/803,1219  
09/803,1220  
09/803,1221  
09/803,1222  
09/803,1223  
09/803,1224  
09/803,1225  
09/803,1226  
09/803,1227  
09/803,1228  
09/803,1229  
09/803,1230  
09/803,1231  
09/803,1232  
09/803,1233  
09/803,1234  
09/803,1235  
09/803,1236  
09/803,1237  
09/803,1238  
09/803,1239  
09/803,1240  
09/803,1241  
09/803,1242  
09/803,1243  
09/803,1244  
09/803,1245  
09/803,1246  
09/803,1247  
09/803,1248  
09/803,1249  
09/803,1250  
09/803,1251  
09/803,1252  
09/803,1253  
09/803,1254  
09/803,1255  
09/803,1256  
09/803,1257  
09/803,1258  
09/803,1259  
09/803,1260  
09/803,1261  
09/803,1262  
09/803,1263  
09/803,1264  
09/803,1265  
09/803,1266  
09/803,1267  
09/803,1268  
09/803,1269  
09/803,1270  
09/803,1271  
09/803,1272  
09/803,1273  
09/803,1274  
09/803,1275  
09/803,1276  
09/803,1277  
09/803,1278  
09/803,1279  
09/803,1280  
09/803,1281  
09/803,1282  
09/803,1283  
09/803,1284  
09/803,1285  
09/803,1286  
09/803,1287  
09/803,1288  
09/803,1289  
09/803,1290  
09/803,1291  
09/803,1292  
09/803,1293  
09/803,1294  
09/803,1295  
09/803,1296  
09/803,1297  
09/803,1298  
09/803,1299  
09/803,1300  
09/803,1301  
09/803,1302  
09/803,1303  
09/803,1304  
09/803,1305  
09/803,1306  
09/803,1307  
09/803,1308  
09/803,1309  
09/803,1310  
09/803,1311  
09/803,1312  
09/803,1313  
09/803,1314  
09/803,1315  
09/803,1316  
09/803,1317  
09/803,1318  
09/803,1319  
09/803,1320  
09/803,1321  
09/803,1322  
09/803,1323  
09/803,1324  
09/803,1325  
09/803,1326  
09/803,1327  
09/803,1328  
09/803,1329  
09/803,1330  
09/803,1331  
09/803,1332  
09/803,1333  
09/803,1334  
09/803,1335  
09/803,1336  
09/803,1337  
09/803,1338  
09/803,1339  
09/803,1340  
09/803,1341  
09/803,1342  
09/803,1343  
09/803,1344  
09/803,1345  
09/803,1346  
09/803,1347  
09/803,1348  
09/803,1349  
09/803,1350  
09/803,1351  
09/803,1352  
09/803,1353  
09/803,1354  
09/803,1355  
09/803,1356  
09/803,1357  
09/803,1358  
09/803,1359  
09/803,1360  
09/803,1361  
09/803,1362  
09/803,1363  
09/803,1364  
09/803,1365  
09/803,1366  
09/803,1367  
09/803,1368  
09/803,1369  
09/803,1370  
09/803,1371  
09/803,1372  
09/803,1373  
09/803,1374  
09/803,1375  
09/803,1376  
09/803,1377  
09/803,1378  
09/803,1379  
09/803,1380  
09/803,1381  
09/803,1382  
09/803,1383  
09/803,1384  
09/803,1385  
09/803,1386  
09/803,1387  
09/803,1388  
09/803,1389  
09/803,1390  
09/803,1391  
09/803,1392  
09/803,1393  
09/803,1394  
09/803,1395  
09/803,1396  
09/803,1397  
09/803,1398  
09/803,1399  
09/803,1400  
09/803,1401  
09/803,1402  
09/803,1403  
09/803,1404  
09/803,1405  
09/803,1406  
09/803,1407  
09/803,1408  
09/803,1409  
09/803,1410  
09/803,1411  
09/803,1412  
09/803,1413  
09/803,1414  
09/803,1415  
09/803,1416  
09/803,1417  
09/803,1418  
09/803,1419  
09/803,1420  
09/803,1421  
09/803,1422  
09/803,1423  
09/803,1424  
09/803,1425  
09/803,1426  
09/803,1427  
09/803,1428  
09/803,1429  
09/803,1430  
09/803,1431  
09/803,1432  
09/803,1433  
09/803,1434  
09/803,1435  
09/803,1436  
09/803,1437  
09/803,1438  
09/803,1439  
09/803,1440  
09/803,1441  
09/803,1442  
09/803,1443  
09/803,1444  
09/803,1445  
09/803,1446  
09/803,1447  
09/803,1448  
09/803,1449  
09/803,1450  
09/803,1451  
09/803,1452  
09/803,1453  
09/803,1454  
09/803,1455  
09/803,1456  
09/803,1457  
09/803,1458  
09/803,1459  
09/803,1460  
09/803,1461  
09/803,1462  
09/803,1463  
09/803,1464  
09/803,1465  
09/803,1466  
09/803,1467  
09

circuit within an IC, but in test configuration it appears as shown in Figure 1. Scan architectures can be applied at various circuit levels. For example, the scan architecture of Figure 1 may represent the testing of a complete IC, or it may represent the testing of an embedded intellectual property core sub-circuit within an IC, such as a DSP or CPU core sub-circuit.

The scan architecture includes an M-bit scan path 101, logic circuitry 102 to be tested, scan input 103, scan output 104, scan enable (SCANENA) 105, scan clock (SCANCK) 106, logic response outputs 107, and logic stimulus inputs 108. During scan testing, a tester or an embedded control circuit in the IC outputs SCANCK and SCANENA control signals to cause scan path 101 to repeat the operations of (1) capturing data from logic 102 via response bus 107, and (2) scanning data through scan path 101 from scan input 103 to scan output 104. During the scan operation, the stimulus outputs 108 from scan path 101 ripple, which causes the inputs to logic 102 to actively change state. Rippling the inputs to logic 102 causes power to be consumed by the interconnect and gating capacitance of the circuits in logic 102.

In Figure 2, a timing diagram example 200 depicts the signals used in the above described scan and capture operations. During scan operation, SCANENA is low from time 204 to 205 and M SCANCKs 201-202 are applied to shift data through the scan path 101. During capture operation, SCANENA is high and a SCANCK 203 is applied to capture response data into the scan path 101. Logical testing of logic 102 is achieved by inputting stimulus and capturing

response. Delay testing of logic 102 is achieved by capturing the response data, via SCANCK 203, immediately following the last scan-in operation that occurs at SCANCK 202. For example, the last shift operation at SCANCK 202 moves or shifts all the stimulus inputs 108 to logic 102 one bit position, which causes the logic 102 to transition to output the final response 107 to scan path 101. The subsequent SCANCK 203 captures this final response transition into scan path 101. Thus the delay test is achieved by having the logic respond to a last stimulus transition during SCANCK 202 to output a last response pattern which is captured into scan path 101 during SCANCK 203. This form of scan path delay testing is well known.

#### Low Power Scan Adaptation Overview

In Figure 3, a low power scan architecture 300 adaptation of the Figure 1 scan path architecture is arranged according to the scan architectures described in the referenced patent Applications Numbers 09/803,588 and 09/803,608. As described in the referenced patent applications, the process of adapting scan architectures for low power operation is advantageously achieved without having to insert blocking circuitry in the stimulus paths, which increases overhead and adds delays, and without having to decrease the scan clock rate which increases test time. Furthermore, as described in the referenced applications, the process of adapting scan architectures for low power operation is advantageously achieved without having to modify the stimulus and response test patterns that are automatically produced by scan architecture synthesis tools.

Adapting the conventional scan path architecture 100 of Figure 1 into the low power scan path architecture 300 of Figure 3 involves reorganizing scan path 101 from being a single scan path containing all the scan cells (M), into a scan path having a desired number of separate scan paths. In Figure 3, scan path 101 is shown after having been reorganized into three separate scan paths A, B, and C 301-303. For simplification, it is assumed that the number of scan cells (M) in the conventional scan path 101 of Figure 1 is divisible by three such that each of the three separate scan paths A, B, and C of Figure 3 contains an equal number of scan cells (M/3).

The serial input of each scan path A, B, and C is commonly connected to scan input 103. The serial output of scan path A is connected to the input of a 3-state buffer 304, the serial output of scan path B is connected to the input of a 3-state buffer 305, and the serial output of scan path C is connected to the input of a 3-state buffer 306. The outputs of the 3-state buffers 304-306 are commonly connected to scan output 104. Scan paths A, B, and C each output an equal number of parallel stimulus inputs (S) to logic 102, and each input an equal number of parallel response outputs (R) from logic 102. The number of stimulus output signals to logic 102 in from the scan architectures in Figures 1 and 3 is the same, and the number of response input signals from logic 102 in Figures 1 and 3 is the same.

Scan paths A-C and buffers 304-306 receive control input from an adaptor circuit which was described in detail

in the referenced patent applications. These control inputs are labeled in Figure 3 as; SCANENA, SCANCK-A, SCANCK-B, SCANCK-C, ENABUF-A, ENABUF-B, and ENABUF-C. Alternatively, these control inputs could be provided from IC pins/pads being driven by a tester, instead of from an adaptor circuit.

In Figure 4, a timing diagram example 400 depicts the operation of the low power scan path of Figure 3. As seen in the timing diagram, each scan operation, which begins at time 401 and ends at time 402, is broken up into a sequence of three sub-scan operations. The first sub-scan operation enables buffer 304 via ENABUF-A and shifts  $M/3$  bits of data through Scan Path A 301 in response to the SCANCK-A's. The second sub-scan operation enables buffer 305 via ENABUF-B and shifts  $M/3$  bits of data through Scan Path B 302 in response to the SCANCK-B's. The third sub-scan operation enables buffer 306 via ENABUF-C and shifts data through Scan Path C 303 in response to the SCANCK-C's. The effect of these sub-scan operations, as previously described in the referenced patent applications, is to reduce the number of simultaneously rippling stimulus inputs to logic 102 from  $M$  in Figure 1 to  $M/3$  in Figure 3. Rippling only portions ( $M/3$ ) of the overall stimulus input ( $M$ ) to logic 102 advantageously reduces power consumption in logic 102 during scan operations.

From the signal timings in Figure 4 it is seen that at the end of the sequence of sub-scan operations, at time 402, the SCANCKs-A, B, and C of Scan Paths A, B, and C are enabled at time 406 to capture response data into Scan Paths A, B, and C. During the sub-scan sequence, Scan Path

A stops shifting data following SCANCK-A at time 403, Scan Path B stops shifting data following SCANCK-B at time 404, and Scan Path C stops shifting data following SCANCK-C at time 405. Since the response capture clock at time 406 occurs immediately after scan clock time 405, the logic portion of logic 102 stimulated by the last shift of Scan Path C does a delay test as described previously in regard to Figure 1 and 2. However, since the response capture clock time 406 does not occur immediately after the last shift time of Scan Path A and C, at times 403 and 404 respectively, it is not possible, with the timing shown in Figure 4, to do delay testing of the logic portions of logic 102 that are stimulated by the last shift operations of Scan Paths A and B.

09055678 09120204

### BRIEF SUMMARY OF THE INVENTION

The present invention provides the addition of a second capture clock at a time that immediately follows the original capture clock.

Alternatively, a first cache bit memory, in this example a D flip flop (FF), can be inserted between the scan input lead and the serial input to scan path A, and a second cache bit memory, again in this example a D flip flop (FF), can be inserted between the scan input lead and the serial input to scan path B. When scan path A is serially loaded, the last bit remains in the first cache bit memory. Likewise, when scan path B is serially loaded, the last bit remains in the second cache bit memory. When scan path C is serially loaded and when the last bit is loaded into the scan path C, the last bits in the first and second cache bit memories are simultaneously loaded into their respective scan paths A and B. This presents the desired stimulus signals to the logic circuits. The next clock signal then captures the response from the logic circuits.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Figure 1 is a block diagram of a scan architecture coupled to a logic circuit in an integrated circuit.

Figure 2 is a timing diagram of signals used in the scan architecture of Figure 1.

Figure 3 is a block diagram of the scan architecture coupled to a logic circuit in an integrated circuit disclosed in the two referenced patent applications.

Figure 4 is a timing diagram of the signals used in the scan architecture of Figure 3.

Figure 5 is a timing diagram of the signals used in the scan architecture of Figure 3 including the additional signals of the present invention.

Figure 6 is a block diagram of a scan architecture coupled to a logic circuit in an integrated circuit that includes the present invention.

Figure 7 is a timing diagram of the signals used in the scan architecture of Figure 6 including the additional signals of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 5 illustrates the timing diagram 500 of Figure 4 modified to allow for delay testing using the low power scan architecture of Figure 3. The modification is simply the addition of a second capture clock at time 407 that immediately follows the original capture clock at time 406. Operating the low power scan architecture of Figure 3 using the timing diagram of Figure 5 enables a delay test of logic 102. The delay test occurs by using the response data captured by the original capture clock at time 406 as delay test stimulus data to produce the response data captured by the second capture clock at time 407. While this approach does provide the previously described low power scan architecture with a delay test capability, it requires that the test patterns, which were originally produced for the conventional scan path architecture of Figure 1, to be modified for use by the low power scan path architecture of Figure 3 when it is operated according to the timing diagram shown in Figure 5. As mentioned in the referenced patent applications, being able to re-use the original test patterns when converting a conventional scan path architecture into a low power scan architecture is a desired objective.

The architecture 600 illustrates how the low power scan path architecture of Figure 3 may be modified into an architecture with a delay test capability that does not require modifying the original test patterns of the conventional scan path architecture of Figure 1. Like the low power scan path architecture of Figure 3, architecture 600 includes a Scan Path A 301, a Scan Path B 302, a Scan

Path C 303, and associated 3-state buffers 304-306 connected to Scan Out 104. Also like the low power scan path of Figure 3, the Scan Paths A, B, and C of Figure 6 are controlled by a SCANENA signal and SCANCK's A, B, and C.

The difference between the low power scan architectures 300 and 600 is that a first cache bit memory, in this example a D flip flop (FF) 601, has been inserted between the Scan Input 103 lead and the serial input to Scan Path A, and a second cache bit memory, again in this example a D flip flop (FF) 605, has been inserted between the Scan Input 103 lead and the serial input to Scan Path B. The D inputs of both FF 601 and 605 are connected to the Scan Input 103. The Q output 604 of FF 601 is connected to the serial input of Scan Path A. The Q output 607 of FF 605 is connected to the serial input of Scan Path B. The clock input 603 of FF 601 is connected to SCANCK-A and the clock input 606 of FF 605 is connected to SCANCK-B.

The timing diagram 700 of Figure 7 illustrates the operation of the low power scan architecture 600 of Figure 6. At time 701, the SCANENA signal goes low to initiate the low power scan operation. From time 703 to time 704, buffer 304 is enabled and M/3 SCANCK-A's shift data through FF 601 and Scan Path A 301 from Scan Input 103 to Scan Output 104. During this shift operation the data contained in Scan Path A is completely shifted out via Scan Output 104. However, during this shift operation, the last bit to be shifted into Scan Path A from Scan Input 103 is left stored in FF 601.

From time 705 to time 706, buffer 305 is enabled and M/3 SCANCK-B's shift data through FF 605 and Scan Path B 302 from Scan Input 103 to Scan Output 104. During this shift operation the data contained in Scan Path B is completely shifted out via Scan Output 104. However, during this shift operation the last bit to be shifted into Scan Path B from Scan Input 103 is left stored in FF 605.

From time 707 to time 708, buffer 306 is enabled and [(M/3)-1] SCANCK-C's shift data through Scan Path C 303 from Scan Input 103 to Scan Output 104. During this shift operation all the data contained in Scan Path C, except for the last data output bit, is shifted out via Scan Output 104. Also during this shift operation, all the data to be loaded into Scan Path C, except for the last input bit, is shifted in via Scan Input 103.

At time 709, buffer 306 remains enabled and all SCANCK's-A, B, and C are activated at once. This simultaneous activation of SCANCK's A, B and C causes; (1) the last scan input bit stored in FF's 601 and 605 to be shifted into Scan Paths A and B respectively, (2) the last input bit from Scan Input 103 to be clocked into Scan Path C, and (3) the last output bit from Scan Path C to be clocked out onto Scan Output 104. This shift operation causes all the stimulus outputs from Scan Path A, B, and C to logic 102 to transition by one bit. Following this shift operation, buffer 306 is disabled.

At time 702 SCANENA goes high to terminate the above described low power shift operation and prepare for the capture operation. At time 710, all SCANCK's A, B, and C

are simultaneously activated to capture the response data from the last shift operation that occurred at time 709. The above described low power shift and capture operations are repeated until the logic 102 has been tested.

Since all stimulus bit inputs to logic 102 transition in response to the simultaneously activated SCANCK's A, B, and C at time 709, the response data captured at time 710 provides a "last shift to capture" delay test which is identical to the "last shift to capture" delay test described previously in regard to the conventional scan path architecture 100. Thus a low power scan architecture with delay test capability is provided by the present invention. The scan and delay test provided by the low power scan architecture 600 can directly re-use the test patterns provided for the conventional scan path architecture 100. Thus the advantage of the low power scan architecture 600 over the low power scan architecture 300 is in its ability to do delay testing using the original test patterns of the pre-adapted conventional scan path architecture 100.

The above process of scanning and capturing data into the low power scan architecture 600 can be summarized in the following steps.

Step 1-Enable Scan Path A\* output, then Do M/3 shifts of Scan Path A\*

Step 2-Enable Scan Path B\* output, then Do M/3 shifts of Scan Path B\*

Step 3-Enable Scan Path C output, then Do [(M/3)-1] shifts of Scan Path C

Step 4-Enable Scan Path C output, then Do one shift of Scan Paths A\*, B\*, & C

Step 5-Capture Response Data into Scan Paths A\*, B\*, & C

Step 6-Repeat Steps 1-5 until test is complete

(Note1: A\* indicates the serial combination of FF 601 and Scan Path A)

(Note2: B\* indicates the serial combination of FF 605 and Scan Path B)

As previously described in the referenced TI patents, the Scan Input 103 can be connected to an IC pin or to an on chip BIST generator circuit, and the Scan Output 104 can be connected to an IC pin or to an on chip BIST compactor circuit.

Also as previously mentioned in the referenced patents, the burst of SCANCK-As, SCANCK-Bs, and SCANCK-Cs occur in a seamless manner such that the scanning of data to and from the low power scan path of circuit 600 via the Scan Input 103 and Scan Output 104 is indistinguishable from the scanning of data to and from the conventional scan path 100 via the Scan Input 103 and Scan Output 104.

The example adaptor circuit described in the referenced patents controlled the low power scan path of architecture 300 by manipulating the SCANCK-A, B, and C signals and the ENABUF-A, B, and C signals according to the timing diagram of Figure 4. To control the low power scan path of architecture 600 according to the timing diagram of Figure 7 and process steps 1-5 listed above, the control

output from the adaptor circuit would need be modified to appropriately manipulate the SCANCK-A, B, and C and ENABUF-A, B, and C signals. If the SCANCK-A, B, C and ENABUF-A, B, C signals were provided at the pins/pads of an IC, then the tester driving the pins/pads would be programmed to control the signals according the timing diagram of Figure 7 and process steps 1-5 listed above.

In architecture 600, it should be clear that, while at least a one bit cache memory is required at the inputs of Scan Path A and B, a multiple bit cache memory could be used at the inputs of Scan Paths A and B as well. For example, if a two bit cache memory were used at the inputs of Scan Path A and B, the above process steps would be maintained with the exception that Steps 3 and 4 would be modified as follows:

Step3-Enable Scan Path C output, then Do  $[(M/3)-2]$  shifts of Scan Path C

Step4-Enable Scan Path C output, then Do two shifts of Scan Paths A\*, B\*, & C

Although the present invention has been described in accordance to the embodiments shown in the Figures, one of ordinary skill in the art will recognize there could be variations to these embodiments and those variations should be within the spirit and scope of the present invention. Accordingly, modifications may be made by one ordinarily skilled in the art without departing from the spirit and scope of the appended claims.